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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/527,569	03/10/2005	Cornelis O. Cirkel	NL02 0843 US	7327

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EXAMINER	
VELEZ, ROBERTO	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/527,569	CIRKEL ET AL.	
	Examiner	Art Unit	
	Roberto Velez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/10/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

   The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 1 and 5 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted step is: in a second step 22, the result of the sampling measurement 20 is considered/analyzed.

   Dependent claims 2-4 and 6-7 are also rejected.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

   A person shall be entitled to a patent unless –

   (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-5 and 7-10 are rejected under 35 U.S.C. 102(e) as being anticipated by ***Ayadi (US Pat. 6,782,331)***.

Regarding claim 1, ***Ayadi*** shows (Figures 1-12) a graphical user interface for testing integrated circuits comprising: generating (using [13, 23]) quality test-data for a limited number of semiconductor devices [44] on the wafer (Column 5, Lines 22-24), deciding (using [13, 23]) based on the generated quality test-data whether other semiconductor devices [44] on the wafer [12] are to be tested (Column 5, Lines 25-34), or not to be tested, based on the result of the deciding step (Column 5, Lines 25-34), testing or not testing (using [20, 40]) the other semiconductor devices [44] on the wafer [12], and (Column 5, Lines 25-37) if some semiconductor devices [44] have not been tested, selecting (using [20, 40]) at least one non- tested semiconductor device [44] on the wafer [12] for further processing.

Regarding claim 2, ***Ayadi*** discloses everything as claimed above in claim 1; in addition, ***Ayadi*** discloses (Column 4, Lines 46-61) wherein the deciding step is a step of automatically deciding based (Column 5, Lines 22-37) on a comparison of a yield calculated from the generated quality test-data, with a pre-set value.

Regarding claim 3, ***Ayadi*** discloses everything as claimed above in claim 1; in addition, ***Ayadi*** shows (Fig. 8) wherein the limited number of semiconductor devices [44] is located on the wafer [12] as determined by a spatial pattern (as shown in Fig. 8).

Regarding claim 4, ***Ayadi*** discloses everything as claimed above in claim 1; in addition, ***Ayadi*** shows (Fig. 8) wherein the pattern comprises a pattern

selected from one or more of a circular pattern, an X-cross pattern, a pattern in the form of a plus sign, a spiral pattern.

Regarding claim 5, ***Ayadi*** shows (Figures 1-12) a graphical user interface for testing integrated circuits on a plurality of wafers (Column 7, Lines 2-3) comprising: generating (using [13, 23]) quality test-data for a limited number of semiconductor devices [44] on a number of wafers (Column 7, Lines 2-3) from the plurality of wafers (Column 5, Lines 22-24), deciding (using [13, 23]) based on the generated quality test-data, for each of the tested wafers (Column 7, Lines 2-3), whether other semiconductor devices [44] on the tested wafers [12] are to be tested (Column 5, Lines 25-34), or not to be tested, based on the result of the deciding step (Column 5, Lines 25-34), testing or not testing (using [20, 40]) the other semiconductor devices [44] on the tested wafers [12], and (Column 5, Lines 25-37) if some semiconductor devices [44] have not been tested, selecting (using [20, 40]) at least one non- tested semiconductor device [44] on the wafer [12] for further processing, wherein the limited number of semiconductor devices [44] on each of the wafers [12] are located on the wafers [12] as determined by a spatial pattern (as shown in Fig. 8), the spatial pattern (as shown in Fig. 8) being such that, by shifting it between wafers [12], a substantially complete wafermap [88] can be obtained.

Regarding claim 7, ***Ayadi*** discloses everything as claimed above in claims 1 and 5; in addition, ***Ayadi*** discloses (Column 1, Lines 11-14) a method for

manufacturing (using 10) a plurality of semiconductor devices [44] on a wafer [12], one of the method steps comprising a step of quality testing.

Regarding claim 8, ***Ayadi*** shows (Fig. 1) a graphical user interface for testing integrated circuits comprising: selecting means [30] for selecting (Column 3, Lines 45-46) a limited number of the plurality of semiconductor devices [44] on the wafer [12] which will be tested, at least one probe [20, 40] for measuring (Column 4, Lines 1-12) whether a selected semiconductor device [44] meets at least one pre-set quality specification, the at least one probe [20, 40] generating quality test results, deciding means [13, 23] for deciding, based on the quality test results, whether other semiconductor devices [44] on the wafer [12] are to be tested or not to be tested.

Regarding claim 9, ***Ayadi*** discloses everything as claimed above in claim 8; in addition, ***Ayadi*** discloses (Column 4, Lines 13-18) wherein the at least one pre-set specifications is a design and/or performance specification.

Regarding claim 10, ***Ayadi*** discloses everything as claimed above in claim 8; in addition, ***Ayadi*** shows (Fig. 1) furthermore comprising a memory means [25, 26] for saving the generated test results.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over ***Ayadi (US Pat. 6,782,331)*** in view of ***Brady et al. (US Pat. 6,236,223)***.

Regarding claim 6, ***Ayadi*** discloses everything as claimed above in claim 5.

Ayadi fails to disclose wherein the shifting of the spatial pattern comprises a rotation of the spatial pattern. However, ***Brady et al.*** shows (Fig. 4A) wherein the shifting of the spatial pattern comprises a rotation of the spatial pattern.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of ***Brady et al.*** into the device of ***Ayadi*** by providing a rotatable stage. The ordinary artisan would have been motivated to modify ***Ayadi*** in the manner set forth above for the purpose of accelerating the testing process by rotating the wafer in order to approach the probe in a faster way.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Alonso Montull et al. (US PGPUB 2002/0121915) shows (Figures 1-6) an automated pattern clustering detection for wafer probe maps.

Naujoks (US Pat. 5,714,888) shows (Figures 1-4) a method and apparatus for testing electronic circuitry in a manufacturing environment.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberto Velez whose telephone number is 571-

272-8597. The examiner can normally be reached on Monday-Friday 8:00am-4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nguyen Ha can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Roberto Velez
Patent Examiner

PARESH PATEL
PRIMARY EXAMINER

04/16/06